Cadence NC-Verilog Simulator Tutorial

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Statements and comments

- Verilog-HDL has a C-like grammar
  - Statements basically end with a semicolon
  - Free format
- Two styles of comments
  - One-line comments
  - Block comments

```
// A one-line comment
/* A block
      comment */
```

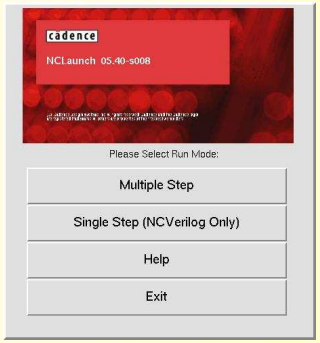
Commands

- CUI tools
  - **ncvlog**: Compiles Verilog files
  - **ncelab**: Elaborates the design and generates a simulation snapshot
  - **ncsim**: Simulates the snapshot
  - **ncverilog**: Single-step invocation
- GUI tool
  - **nclaunch**

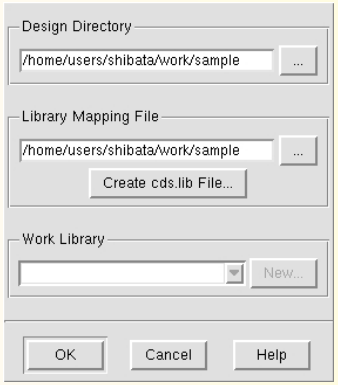
Starting NCLaunch

```
% nclaunch -new &
```

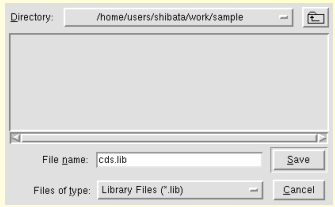
- The *-new* option is required for a new design
- Click *Multiple Step*



Setting up libraries (1/2)

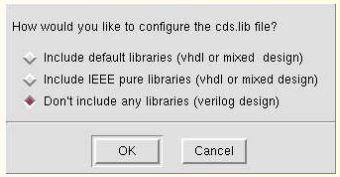


- Click *Create cds.lib File*

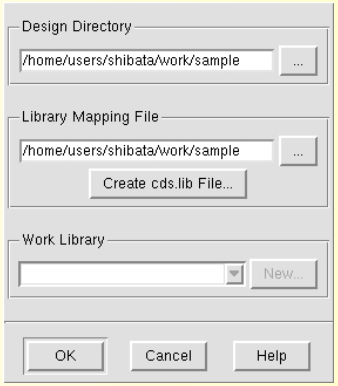


- Click *Save*

Setting up libraries (2/2)



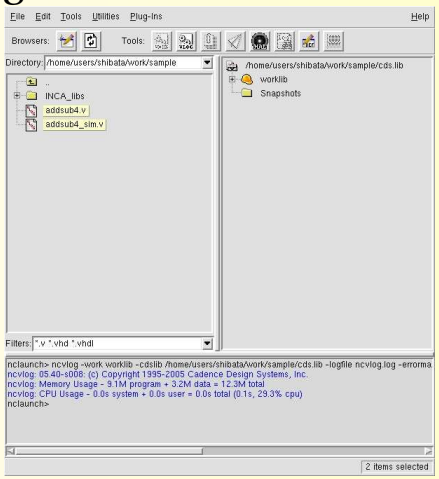
- Select *Don't include any libraries* and click *OK*



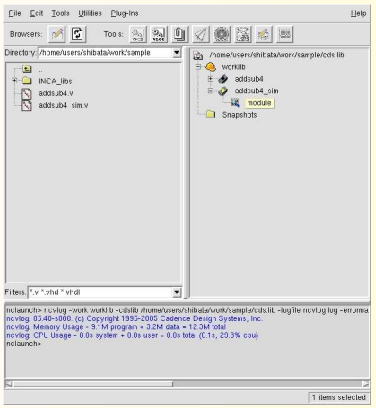
- Click *OK*

Compiling the source files

- Select the source files (Ctrl+click selects multiple files)
- Click the *Verilog Compiler* button

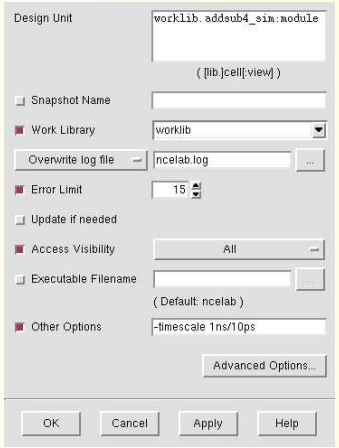


Elaborating the design



- Expand *workilib*
- Expand the top-level design unit (here, *addsub4_sim*)
- Select module
- Choose *Tools* --> *Elaborator*

Elaborating the design (2/2)

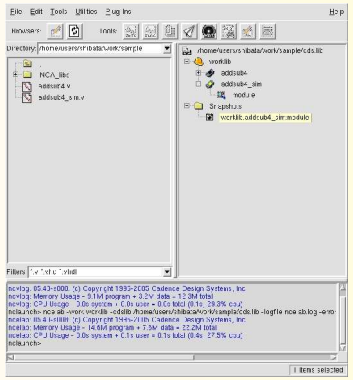


- Enable *Other Options* button and enter the following option

```
-timescale 1ns/10ps
```

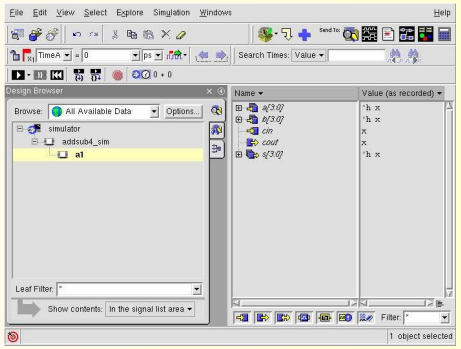
- Click *OK*

Starting the simulator



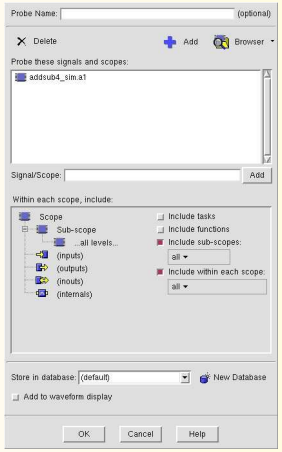
- Expand the *snapshots* folder
- Select the snapshot you want to simulate
- Click *Simulator* button
- After invoking the simulator,
  - Chose *File --> Exit* to exit NCLaunch

Selecting the data to save



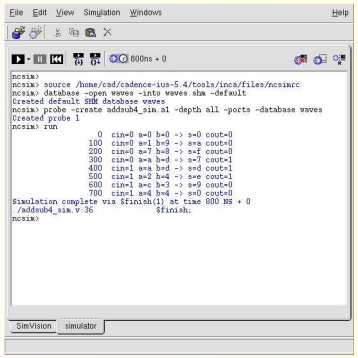
- In Design Browser, expand the top module
- Select the scope you want to probe (here, *a1*)
- Choose *Simulation --> Create Probe*

Selecting the data to save



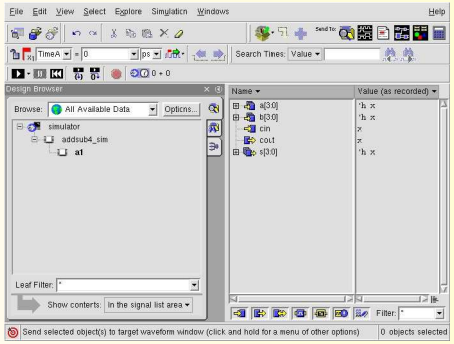
- Select the objects you want to probe
  - Enable *Include sub-scopes* and set to *all*
  - Enable *Include within each scope* and set to *all*
- Disable *Add to wave form display*
- Click *OK*

Starting the simulation



- Choose Simulation --> Run
- Messages appear in the *simulator* tab in the *Console* window

Opening a waveform window

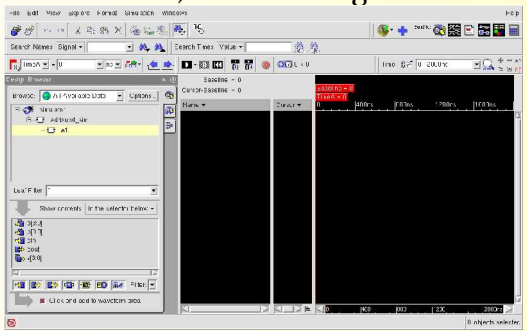


- In Design Browser, deselect any scopes (with Ctrl+click)
- Click the *waveform* button

Selecting the signals to see

- In *Waveform* window, expand the sidebar:

- Expand and select the scope
- In the select area, select the signals



Selecting the signals to see

- Collapse the sidebar